CLAIMS

What is claimed is:

1. A data buffer, the data buffer comprising:

an entry section; and

a signaling circuit coupled to the entry section for providing a signal to transfer a portion of a data cell from the entry section prior to the data cell being completely received by the entry section.

2. The data buffer of claim 1 wherein the signal is provided once the amount of data received by the entry section reaches a predetermined threshold.

3. The data buffer of claim 2 wherein the entry section comprises a buffer entry section.

4. The data buffer of claim 3 wherein the signaling circuit comprises an asynchronous signaling circuit.

5. The data buffer of claim 4 wherein the buffer entry section comprises a write element and a read element, wherein the write element and the read element each comprise an entry pointer, an item pointer and an entry counter.

6. The data buffer of claim 5 wherein the asynchronous signaling circuit comprises an add signaling portion and a remove signaling portion.

7. The data buffer of claim 6 wherein the asynchronous signaling circuit provides a signal to the write element to begin writing another data cell into the buffer entry section prior to the data cell being completely read from the buffer entry section wherein the signal is provided based on a predetermined threshold.

8. A data buffer for buffering a data cell, the data buffer comprising:

a buffer entry section including a write element and a read element, wherein the write element and the read element each comprise an entry pointer, an item pointer and an entry counter; and

an asynchronous signaling circuit coupled to the buffer entry section, wherein the asynchronous signaling circuit provides a first signal to the read element to transfer data from the buffer entry section prior to a data cell being completely received by the buffer entry section wherein the signal is provided once the amount of data received by the buffer entry section reaches a predetermined threshold.

9. The data buffer of claim 8 wherein the asynchronous signaling circuit comprises an add signaling portion and a remove signaling portion.

10. The data buffer of claim 9 wherein the asynchronous signaling circuit provides a second signal to the write element to begin writing another data cell into the buffer entry section prior to the data cell being completely read from the buffer entry section wherein the second signal is provided once the amount of data received by the buffer entry section reaches

a predetermined threshold.

11. A data buffer for buffering a data cell, the data buffer comprising:

a buffer entry section including a write element and a read element, wherein the write element and the read element each comprise an entry pointer, an entry counter and an item pointer; and

an asynchronous signaling circuit coupled to the buffer entry section, the asynchronous signaling circuit comprising an add signaling portion and a remove signaling portion, wherein the asynchronous signaling circuit provides a first signal to the read element prior to the data cell being completely written into the buffer entry section and a second signal to the write element prior to the data cell being completely read from the buffer entry section, wherein the first signal is provided once the amount of data received by the buffer entry section reaches a predetermined threshold and the second signal is provided once the amount of data read from the buffer entry section reaches a predetermined threshold.

12. A method of transferring data in a data buffer, the method comprising the steps of:

a) allowing a data cell to begin being written into the data buffer; and

b) reading the data cell from the data buffer prior to the data cell being completely written into the data buffer.

13. The method of claim 12 further comprising:

c) allowing another data cell to begin being written into the data buffer

prior to the data cell being completely read out of the data buffer.

14. The method of claim 13 wherein the data cell comprises a plurality of portions and the data buffer comprises:

a buffer entry section including a write element and a read element; and

an asynchronous signaling circuit coupled to the buffer entry section.

SUBAIT

15. The method of claim 14 wherein the asynchronous signaling circuit comprises an add signaling portion and a remove signaling portion.

16. The method claim 15 wherein the write element comprises a first entry pointer, a first item pointer, and a first entry counter and the read element comprises a second entry pointer, a second item pointer and a second entry counter.

17. The method of claim 16 wherein step a) further comprises:

a1) allowing the write element to write each of the plurality of data cell portions to the buffer entry section via an access to the buffer entry section;

a2) incrementing the first item pointer each time the buffer entry section is accessed; and

a3) allowing the asynchronous signaling circuit to provide a signal to the read element once the first item pointer reaches a predetermined threshold.

18. The method of claim 17 wherein the signal of step a3) comprises an add signal.

19. The method of claim 18 wherein step a) further comprises:

a4) incrementing the second entry counter.

20. The method of claim 16 wherein step b) further comprises:

b1) allowing the read element to receive a signal from the asynchronous signaling circuit;

b2) allowing the read element to read each of the plurality of data cell portions from the buffer entry section via an access to the buffer entry section;

b3) incrementing the second item pointer each time the buffer entry section is accessed; and

b4) allowing the asynchronous signaling circuit to provide a signal the write element once the second item pointer reaches a predetermined threshold.

21. The method of claim 20 further comprising:

b5) decrementing the first entry counter.

22. The method of claim 21 wherein the signal of step b1) comprises an add signal and the signal of step b4) comprises a remove signal.